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GROWTH OF STEP-FREE SURFACES ON DEVICE-SIZE (0001) SiC MESAS

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Abstract. It is believed that atomic-scale surface steps cause defects in single-crystal films grown heteroepitaxially on SiC substrates. A method is described whereby surface steps can be grown out of existence on arrays of device-size mesas on commercial ‘‘on-axis’’ SiC wafers. Step-free mesas with dimensions up to 200 mm square have been produced on 4H-SiC wafers and up to 50 mm square on a 6H-SiC wafer. A limiting factor in scaling up the size and yield of the step-free mesas is the density of screw dislocations in the SiC wafers. The fundamental significance of this work is that it demonstrates that two dimensional nucleation of SiC can be suppressed while carrying out step-flow growth on (0001) SiC. The application of this method should enable the realization of improved heteroepitaxially-grown SiC and GaN device structures.

1. INTRODUCTION

Single crystals of the hexagonal polytypes of silicon carbide(SiC) are being used as substrates for the growth of heteroepitaxial films. Important commercial applications include the growth of GaN on SiC for the fabrication of shortwavelength light emitting diodes, laser diodes, and heterojunction radio frequency transistors. The GaN films contain a very high density of defects (typically 10^9 cm^{-2}). The polished surface of ‘‘on-axis’’ commercial SiC wafers, frequently used for heteroepitaxy, is usually within 0.3° of the (0001) basal plane. In the case of 3C-SiC grown on 6H-SiC, surface steps lead to double-positioning boundaries in the 3C films. Surface steps may also play a role in the nonideal electrical performance of SiC inversion-channel metal–oxide–semiconductor field effect transistors (MOSFETs).

2. GROWTH OF STEP-FREE SURFACES ON SIZE (0001) SiC

Figure 1 illustrates in a simplified fashion our process for achieving step-free SiC surfaces. Figure 1(a) illustrates the surface steps present on the initial on-axis wafer surface due to the small tilt angle between the basal plane and the polished surface. Commercially available on-axis SiC wafers have a high surface step density. An on-axis wafer with a typical 0.3° tilt angle (relative to the basal plane) will have surface steps with a terrace width of 50 nm, assuming a 0.25 nm step height (the height of a SiC bilayer). The first step in the process is to etch an array of mesas on the SiC wafer top surface. Then homoepitaxial growth is carried out on the mesas under conditions (described in the next paragraph) that promote step-flow growth while at the same time suppressing 2D nucleation on the mesa tops. In this manner, the atomic steps on each mesa top grow themselves out of existence, leaving a basal plane surface (tilted with respect to the original surface), as illustrated in Fig. 1(b). In idealized conditions where 2D terrace nucleation is completely suppressed, there will be no further growth perpendicular to the basal plane.

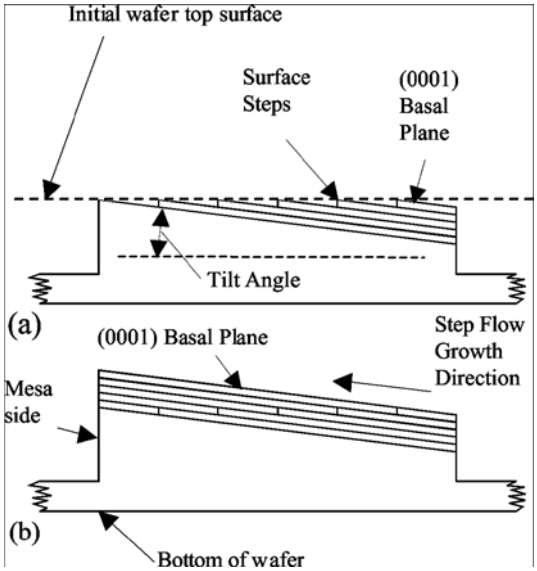

FIG. 1. Schematic diagram illustrating the growth of step-free mesas. (a) Before growth initial mesa surface (parallel to bottom of wafer surface) contains steps due to tilt of basal plane with respect to polished wafer surface. (b) After growth, steps have been grown out of existence, leaving a step-free mesa surface parallel to the basal plane (i.e., tilted with respect to the initial surface).

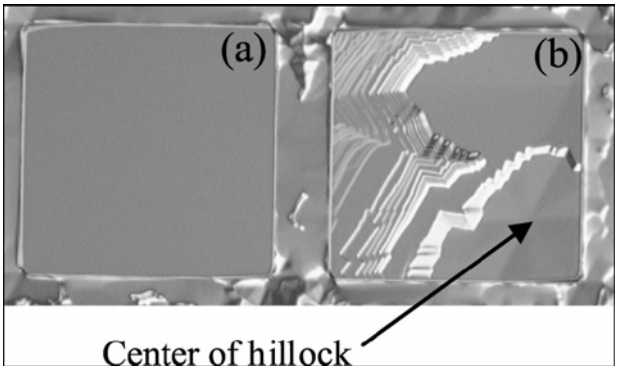

FIG. 2. Optical (Nomarski) images of two adjacent 200 mm square mesas on a 4H-SiC wafer. Mesa (a) (left) is step-free and mesa (b) (right) Contains a screw dislocation which provided a continuous source of steps during growth.

For simplicity, growth that occurs on the mesa sidewall and bottom of the grooves is not shown in Fig 1(b).

To demonstrate the process, three commercially purchased on-axis SiC wafers were used (two 4H and one 6H). On the polished Si face of each wafer, mesas were fabricated by etching 5 μm deep grooves using an inductively coupled plasma etch system. The indium tin oxide mesa mask contained square mesa patterns with the sizes 50, 100, 200, 300, and 400 μm. The epitaxial growth was carried out in a commercial single-wafer chemical vapor deposition system with an inductively heated uncoated graphite susceptor. Each wafer separately underwent an epitaxial growth process consisting of (1) an *in situ* H_2 etch for 5 min at 1600 °C at a pressure of 100 mbar followed by (2) a growth for 30 min at 1600 °C at a pressure of 200 mbar. The sources of Si and C were SiH_4 (2.7 cm^3 /min) and C_3H_8 (0.3 cm^3/min), respectively, in H_2 (total flow 4400 cm^3/min). Neither the etch nor the epitaxial growth parameters were optimized.

Following growth runs, the three SiC wafer surfaces were examined optically (Nomarski differential interference contrast) and by atomic force microscopy (AFM).

Growth was observed on the mesa tops and sidewalls as well as the bottom of the grooves. All three wafers exhibited step-free mesas; however, one of the two 4H wafers yielded a higher percentage of step-free mesas than the other two wafers. From the optical observations, nearly all of the mesa top surfaces on the 4H wafers exhibited one of three characteristics: (1) the surface was featureless, (2) the surface contained at least one hexagonal hillock which dominated the growth morphology, or (3) for a small percentage of mesas there were several large featureless regions separated by lines. For an unknown reason, hillocks were more difficult to discern with the optical microscope on the 6H mesa surfaces, compared with the 4H mesas; however, using moderate magnification (e.g., 100X), hillocks could be discerned on surfaces of both polytypes.

For the better of the two 4H wafers, most of the 50 and 100 μm mesas were optically featureless. All of the 300 and 400 μm mesas contained at least one hillock. Although most 200 μm mesas contained hillocks, there were tens of these mesas over the whole 50 μm wafer that were featureless. Figure 2 is an optical image of a 4H wafer showing two adjacent 200 μm mesas. Mesa (a) on the left is featureless and mesa (b) on the right contains a hillock which dominates the surface morphology.

AFM scans of the two 200 μm mesas of Fig. 2 are presented in Fig. 3. Figure 3(a) is one of sixteen 50 μm square scans of mesa (a) that were recorded in order to cover the entire 200 μm square mesa. No atomic steps or other features were observed in any of the 16 scans. Some parallel lines were observed in the scans at the left and right sides of the mesa, but these were attributed to artifacts of the measurement. This conclusion was reached since the parallel lines remained along the left and right sides of the AFM image even when the sample was rotated 90° (i.e., the lines did not follow the rotation of the sample). Such interference effects have been reported by other AFM users while observing extremely flat surfaces. In this particular case, it appears that the interference fringes were mostly due to the mesa edge.

Figure 3(b) shows the center of the hillock of mesa (b). The well-defined steps (0.5 and 1.0 nm high) seen in this image, emanating from the center, are produced by a screw dislocation. The morphology and step height measurement indicates a screw dislocation with a 1 nm Burgers vector in the *c*-axis direction. This is consistent with an elementary screw dislocation in 4H-SiC. Since the smallest step possible on a (0001) SiC surface is the height of a single bilayer (0.25 nm), it is clear that the AFM can detect any steps that may be present on the mesas.

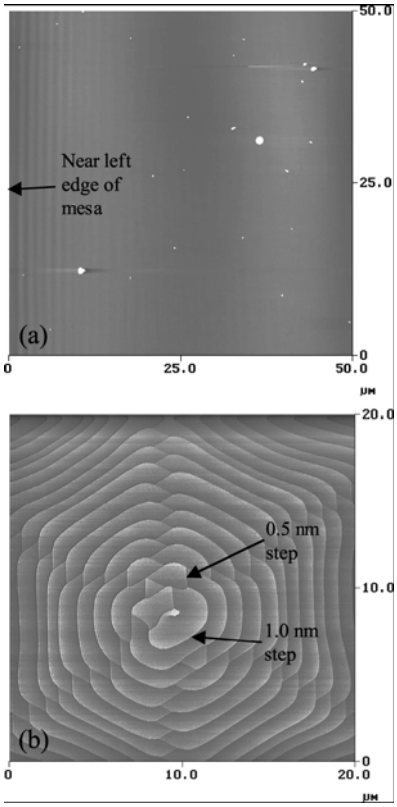

FIG. 3. AFM images of the two mesas of Fig. 2. (a) 50 μm scan near the left edge of step-free mesa A. (b) 30 mm scan of steps emanating from center of the screw dislocation in mesa B. Images have been ''flattened'' in order to show steps across entire scanned area. White ''dots'' are particles on surface.

Additional AFM scans (30 μm square) were recorded for twenty-two 50 μm mesas on the better 4H wafer. Hillocks had been observed on only two of these mesas by the optical microscope; the remaining were optically featureless. The AFM scans confirmed that each of the two mesas with hillocks had steps due to screw dislocations, and of the remaining 20 optically featureless mesas, 18 were totally stepfree while two mesas each had large step-free areas separated by stepped boundaries.

Examination of the 6H wafer yielded the following result. The only optically ''featureless'' mesas were a small percentage of the 50 μm mesas. An AFM examination of 8 of these featureless 50 μm mesas demonstrated that seven were step-free. An examination of 12 randomly selected 50 nm mesas yielded only one step-free mesa. Most of the remaining 11 had hillocks generated by elementary screw dislocations, with step heights of 0.75 and 1.5 nm.

Some comments and conclusions from the previously mentioned observations are the following. It appears that the major determining factor in obtaining a step-free mesa was whether the mesa contained a screw dislocation. In almost every case, if a mesa contained a screw dislocation, then (1) *existing* surface steps (created by the off-cut tilt angle) Would be grown out of existence by step-flow growth, and (2) *New* steps would be generated by the screw dislocation. The new steps dominate the mesa morphology. It had been expected that contamination and defects generated by polishing damage would play a greater role in determining mesa morphology. We conclude that the maximum size and yield of stepfree mesas on a wafer is primarily limited by the density of screw dislocations in the wafer. For example, a uniform screw dislocation density of 10^4 cm^{-2} would produce an average of one dislocation for each 100 μm square (10^{-4} cm^2) area! mesa. Based on the high yield of step-free 100 μm square mesas on the better of the two 4H wafers, the

dislocation density in that wafer is estimated to be less than 10^4 cm^{-2} . The dislocation density in the 6H wafer appears to be much higher than 10^4 cm^{-2} . We do not know whether this higher dislocation density is typical of commercially available 6H wafers.

3. CONCLUSIONS

The process described in this letter provides step-free mesa surfaces that are isolated from mesas with steps associated with screw dislocations. Hence, the step-free 100 and 200 μm square mesas that can be produced will be very useful in evaluating the suitability of step-free SiC surfaces for the heteroepitaxial growth of low-defect single-crystal films of wide-band gap semiconductor compounds such as 3C-SiC, AlN, and GaN. If greatly improved wide-band gap heteroepitaxy can be realized on these step free surfaces, this in turn may enable new and/or greatly improved wide-band gap device structures, ranging from better-performing 3CSiC diodes and transistors to previously unrealizable heterojunction FET and heterojunction bipolar transistor devices based on (Al)GaN/SiC and/or beta-SiC/alpha-SiC heterojunctions. One can also speculate that step-free SiC surfaces may enable fabrication of SiC MOSFETs and Schottky diodes with greatly reduced interface surface roughness, which may lead to improved device performance and reliability. The high yield achieved for the 100 μm square mesas is dependent on the *area* of the mesa. One should be able to obtain a high yield for other mesa shapes of equivalent area; for example, a 20 μmX500 μm mesa. Hence, the present yield should allow fabrication of laser diode structures and other semiconductor devices with arbitrary shapes.

BIBLIOGRAPHY

[1] Aixtron Inc. Model AIX 200/4 HT.
[2] Beheim G. M. and Salupo C. S., Mater. Res. Soc. Symp. Proc.
[3] Chernoff D. A. and Magonov S.
[4] Digital Instruments Model Dimension 3000.
[5] Dudley W. Si, M., Glass R., V. Tsvetkov, and C. H. Carter, Jr., J. Electron. Mater. **26**, 128 (1997). Appl. Phys. Lett., Vol. 77, No. 10, 4 September 2000 Powell et al. 1451
[6] Edmond J., Bulman G., H. S. Kong, M. Leonard, K. Doverspike, W. Weeks, J. Niccum, S. T. Sheppard, G. Negley, D. Slater, J. D. Brown, J. T. Swindell, T. Overocker, J. F. Schetzina, Y.-K. Song, M. Kuball, and A. Nurmikko, in *International Conference on Silicon Carbide and Related Materials, 1997*, edited by G. Pensl, H. Morkoc, B. Monemar, and E. Janzen ~Trans Tech, Stockholm, Sweden, 1998!, Vol. 264–268, pp. 1421–1424.
[7] Hanser A. D. and Davis R. F., in *Gallium Nitride and Related Semiconductors*, edited by J. H. Edgar, S. Strite, I. Akasaki, H. Amano, and C. Wetzel ~Short Run, Exeter, 1999!, pp.386 390.
[8] Nishida T. and Kobayashi N., Jpn. J. Appl. Phys., Part 2 **37**, L13 ~1998!.
[9] Ouisse T., Phys. Status Solidi A **162**, 339 ~1997!.
[10] Powell J. A., Petit J. B., J. H. Edgar, I. G. Jenkins, L. G. Matus, J. W. Yang, P. Pirouz, W. J. Choyke, L. Clemen, and M. Yoganathan, Appl. Phys. Lett. **59**, 333 ~1991!.
[11] Powell J. A., Larkin D. J., P. G. Neudeck, and L. G. Matus, US Patent No. 5,915,194 ~June 22, 1999!.
[12] Tanaka S., Kern R. S., and R. F. Davis, Appl. Phys. Lett. **66**, 37 ~1995!.